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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/876,292	06/07/2001	Mahalingam Nandakumar	TI-31089	9537

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EXAMINER	
ORTIZ, EDGARDO	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

RF

Office Action Summary

Application No.	Applicant(s)
09/876,292	Nandakumar Et.al.
Examiner	**Art Unit**
Edgardo Ortiz	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jun 23, 2003*.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-11* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☒ The proposed drawing correction filed on *Apr 1, 2003* is: a) ☒ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This Office Action is in response to a request for reconsideration filed June 23, 2003.

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-11 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-13 of Nadakumar et.al. (U.S. Patent No. 6,452,236) in view of Arimura et.al. (U.S. Patent No. 5,449,937). With regard to Claim 1 of the instant application, claim 1 of U. S. Patent No. 6,452,236 discloses an integrated circuit fabricated in a semiconductor of a first conductivity type, said circuit having at the surface at least one lateral MOS transistor bordered on each side by an isolation region and below said surface by a channel stop region, comprising a source and a drain each comprising at said surface two regions of the opposite conductivity type, one of said regions shallow and extending to the transistor gate, the other of said regions deeper and recessed from said gate, together defining the active area of said transistor and having a depletion region when reverse biased, another semiconductor region of said first conductivity, having a resistivity higher than the remainder of said semiconductor, extending laterally approximately from the inner border of the respective shallow region to the inner border of the respective recessed region, since claim 1 of U.S. Patent No. 6,452,236 discloses that the "another semiconductor region" extends from the "vicinity" of the recessed region to the "vicinity" of the other or shallow region, wherein "vicinity" inherently includes the inner borders, and said high resistivity regions extending vertically from a depth just below the depletion regions of said source and drain to approximately the top of said channel stop region.

However, claim 1 of U. S. Patent No. 6,452,236 fails to teach that the shallow regions are surrounded by an enhanced doping implant region of the first conductivity type and high resistivity regions within said enhanced doping implant region. Arimura discloses field effect transistor including n-type source and drain regions (13s, 13d), n-type lightly-doped regions (11s, 11d) and p-type enhanced doping implants (10) surrounding the lightly-doped regions. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by claim 1 of U. S. Patent No. 6,452,236 to include first conductivity type enhanced doping implant regions that inherently contain high resistivity regions and which surround shallow regions of an opposite conductivity type, as clearly suggested by Arimura, in order to suppress short-channel effect (column 5, lines 9-10).

With regard to Claim 2 of the instant application, claim 2 of U. S. Patent No. 6,452,236 discloses a semiconductor of the first conductivity type that is a semiconductor epitaxial layer.

With regard to Claim 3 of the instant application, claim 3 of U. S. Patent No. 6,452,236 discloses a semiconductor material that is selected from a group consisting of silicon, silicon germanium, gallium arsenide and any other semiconductor material used in integrated circuit fabrication.

With regard to Claim 4 of the instant application, claim 4 of U. S. Patent No. 6,452,236 discloses regions of higher resistivity within the semiconductor of the first conductivity type that have a

resistivity at least an order of magnitude then the resistivity of said semiconductor of the first conductivity type.

With regard to Claim 5 of the instant application, claim 5 of U. S. Patent No. 6,452,236 discloses depletion regions that have a depth of about 40 to 50 nm from said surface so that the high resistivity regions extend vertically from about 50 to 150 nm from said surface.

With regard to Claim 6 of the instant application, claim 6 of U. S. Patent No. 6,452,236 discloses a semiconductor of the first conductivity type that is made of p-type silicon in the resistivity range from about 1 to 50 Ωcm and the source, drain and their extensions are made of n-type silicon.

With regard to Claim 7 of the instant application, claim 7 of U. S. Patent No. 6,452,236 discloses a semiconductor of the first conductivity type that has a dopant species selected from a group consisting of boron, aluminum, gallium and indium, while said source, drain, their extensions and said semiconductor of the first conductivity type have a dopant species selected from a group consisting of arsenic, phosphorus, antimony and bismuth.

With regard to Claim 8 of the instant application, claim 8 of U. S. Patent No. 6,452,236 discloses a semiconductor of the first conductivity type that is made of n-type silicon in the resistivity

range from about 1 to 50 Ωcm and the source, drain and their extensions are made of p-type silicon.

With regard to Claim 9 of the instant application, claim 9 of U. S. Patent No. 6,452,236 discloses a semiconductor of the first conductivity type that has a dopant species selected from a group consisting of arsenic, phosphorus, antimony, bismuth and lithium, while said source, drain , their extensions and said regions of higher resistivity within said semiconductor of the first conductivity type have a dopant species selected from a group consisting of boron, aluminum, gallium, indium and lithium.

With regard to Claim 10 of the instant application, claim 10 of U. S. Patent No. 6,452,236 discloses a gate that has a narrow dimension from about 0.2 to 1.0 μm, thus smaller than about 0.2 μm.

With regard to Claim 11 of the instant application, claim 13 of U. S. Patent No. 6,452,236 discloses regions of higher resistivity that improve the ESD protection of the transistor without decreasing lath-up robustness or increasing inadvertent substrate current-induced body biasing of neighboring transistors. However, claim 13 of U. S. Patent No. 6,452,236 does disclose that the higher resistivity regions enhance the gain of the lateral bipolar transistor and the current needed for initiating thermal breakdown. It would be obvious to someone with ordinary skill in the art

that these two conditions are inherently obtained with the structure as taught by U. S. Patent No. 6,452,236, since the claimed invention does not structurally or patentably distinguish from that taught by the reference.

Response to Arguments

3. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Edgardo Ortiz (Art Unit 2815), whose telephone number is (703) 308-6183 or by fax at (703) 308-7724. In case the Examiner can not be reached by a direct telephone call, you might call Supervisor Eddie Lee at (703) 308-1690. Any inquiry of a general nature or relating to the status of this application should be directed to the Group 2800 receptionist whose telephone number is (703) 308-0956.

EO / AU 2815

9/15/03

GEORGE ECKERT
PRIMARY EXAMINER